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EXAMINER	
SCHEIBEL, ROBERT C	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/046,566	CHOW, FELIX	
	Examiner	Art Unit	
	Robert C. Scheibel	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 37-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 37-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

- Examiner acknowledges Applicant's Amendment filed 4/10/2006.
- Claims 16-36 have been cancelled.
- New claims 37-50 have been added.
- Claims 1-15 and 37-50 are currently pending.

Response to Arguments

1. Applicant's arguments, see page 11, filed 4/10/2006, with respect to the objections to the drawings have been fully considered and are persuasive. The objections to the drawings have been withdrawn.

2. The previous objection to claim 33 has been withdrawn as claim 33 has been cancelled in the present amendment.

3. Applicant's arguments, see page 12, filed 4/10/2006, with respect to the rejection of claims 16-22, 25-28, and 31-36 under 35 U.S.C. 102(e) have been fully considered and are persuasive. The arguments indicated that said claims have been cancelled. Therefore, the rejection of claims 16-22, 25-28, and 31-36 under 35 U.S.C. 102(e) has been withdrawn.

Claim Objections

4. Claims **44 and 47** are objected to because of the following informalities: the phrase "said first clock cycle" in lines 6-7 should be changed to "a first clock cycle" as there is no first clock cycle earlier in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims **1-14 and 47-49** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication 2002/0176449 to Trippe in view of U.S. Patent 5,081,654 to Stephenson, Jr. et al.

Regarding claim **1**, Trippe discloses a method of parallel processing bit-synchronous HDLC data (see lines 1-5 of paragraph 23 on page 2), comprising: storing at least two bytes of bit-synchronous HDLC data (lines 6-8 of paragraph 26 on page 2 and figure 2, for example, which indicates that 16 or more bits are stored and processed at once); processing in parallel (see lines 1-5 of paragraph 23 on page 2) a plurality of bits within said shift register so as to detect a SOF sequence during a first clock cycle (see lines 9-12 of paragraph 7 on page 1 and paragraph 35 of page 3, for example; the "start-of-frame" is the SOF sequence referred to in the claim; see also lines 3-5 in paragraph 25 on page 2 which indicates that the processing of the multiple bits occurs in a single clock cycle); processing in parallel a plurality of bits within said shift register so as to detect an EOF sequence during at least one subsequent clock cycle (see lines 9-12 of paragraph 7 on page 1 and paragraph 35 of page 3, for example; the "end-of-frame" is the EOF sequence referred to in the claim; see also lines 3-5 in paragraph 25 on page 2 which indicates that the processing of the multiple bits occurs in a single clock cycle); and sending valid payload data bits to a packer logic unit (bit accumulator 338 in figure 5, for example),

wherein said valid payload data bits comprise at least some bits shifted into said shift register between said SOF sequence and said EOF sequence (see paragraphs 37-38 and 40 on page 3 which indicates how the received data is that which is received between the start or end flags).

Similarly, regarding claim **6**, Trippe discloses a method of parallel processing bit-synchronous data (see lines 1-5 of paragraph 23 on page 2), comprising: storing at least two bytes of bit-synchronous data (lines 6-8 of paragraph 26 on page 2 and figure 2, for example, which indicates that 16 or more bits are stored and processed at once); processing in parallel a plurality of bits within said shift register so as to detect valid payload data bits (see paragraphs 37-38 and 40 on page 3 which indicates how the received data is that which is received between the start or end flags); and storing detected valid payload data bits in a packer logic unit (bit accumulator 338 in figure 5, for example) for further processing (see paragraph 41 on page 3 which indicates some of the further processing).

Similarly, regarding claim **47**, Trippe discloses a bit-synchronous HDLC engine (see title and lines 1-5 of paragraph 23 on page 2), comprising: a register for storing at least two bytes of bit-synchronous HDLC data (lines 6-8 of paragraph 26 on page 2 and figure 2, for example, which indicates that 16 or more bits are stored and processed at once); and a de-framer unit (the flag/abort detector 330 of figure 5, for example), coupled to said shift register, for detecting valid payload data within said shift register, said de-framer unit detects a SOF sequence during said first clock cycle (see lines 9-12 of paragraph 7 on page 1 and paragraph 35 of page 3, for example; the "start-of-frame" is the SOF sequence referred to in the claim; see also lines 3-5 in paragraph 25 on page 2 which indicates that the processing of the multiple bits occurs in a single clock cycle) and detects an EOF sequence during a subsequent clock cycle (see lines 9-12 of

paragraph 7 on page 1 and paragraph 35 of page 3, for example; the "end-of-frame" is the EOF sequence referred to in the claim; see also lines 3-5 in paragraph 25 on page 2 which indicates that the processing of the multiple bits occurs in a single clock cycle), said valid payload data comprises at least some of the bits received between said SOF sequence and said EOF sequence (see paragraphs 37-38 and 40 on page 3 which indicate how the received data is that which is received between the start or end flags); and a packer logic unit, coupled to said de-framer unit, for storing said valid payload data received from said de-framer unit (bit accumulator 338 and bit shifter 336 in figure 5), wherein said packer logic unit discards said valid payload data received from said de-framer unit if an amount of valid payload data bits received constitute less than a minimum number (N) of bytes (see paragraph 41 on page 3 which indicates that the accumulator outputs the unframed (destuffed) bits in n-bit batches; clearly, if less than this number of bits is stored in the accumulator when a framing byte is detected, these bits are discarded since the accumulator only outputs n-bit batches).

Trippe does not disclose expressly the limitation that the HDLC data is stored in a shift register, wherein, at each successive clock cycle, a new incoming byte is shifted into said shift register and an old byte is shifted out of said shift register of claim 1. Similarly, Trippe does not disclose the limitation of claim 6 that the bit-synchronous data is stored in a shift register, wherein a newly received byte is shifted in and an old byte is shifted out of said shift register at each clock cycle. Trippe also does not disclose the limitation that the register for storing at least two bytes of claim 47 is a shift register or that a new byte is shifted in and an old byte is shifted out of said shift register during each successive clock cycle. Trippe does not disclose the limitation of claim 47 that said de-framer unit comprises a plurality, of comparators for detecting

a specified sequence of bits within said shift register during a first clock cycle, wherein each comparator is coupled to a unique subset of eight successive bits contained within said shift register.

Stevenson, Jr. discloses the limitations of claims 1, 6, and 47 of a shift register wherein at each successive clock cycle, a new incoming byte is shifted into said shift register and an old byte is shifted out of said shift register in lines 9-24 of column 6. Specifically, the passage starting on line 15 indicates that each data word causes the previous data words to be shifted over one latch. Stevenson, Jr. further discloses the limitation that the de-framer unit comprises a plurality, of comparators for detecting a specified sequence of bits within said shift register during a first clock cycle, wherein each comparator is coupled to a unique subset of eight successive bits contained within said shift register in lines 24-49 of column 6 and in the example of figure 6. Clearly, successive 8-bit sequences of bits are scanned simultaneously to detect a given word (framing byte in this case).

Trippe and Stevenson, Jr. are analogous art because they are from the same field of endeavor of detecting byte patterns in bit sequences. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Trippe by using the shift registers (latches) to store the HDLC data while it is being analyzed and to further use the detectors as described by Stevenson, Jr. to simultaneously look at all successive 8-bit sequences in this shift register.

The motivation for doing so would have been allow the 8-bit framing bytes (SOF, EOF) to be detected regardless of the starting bit location of that byte as suggested by Stevenson, Jr. in lines 44-49 of column 6. Therefore, it would have been obvious to combine Stevenson, Jr. with

Trippe for the benefit of detecting framing bytes regardless of the starting bit location to obtain the invention as specified in claims 1, 6, and 47.

Regarding claims **2 and 48**, Trippe discloses processing in parallel a plurality of bits within said shift register to detect an Abort sequence during said at least one subsequent clock cycle, wherein if said Abort sequence is detected, all bits received after said SOF sequence are discarded and a search for a new SOF sequence is initiated in paragraph 38 on page 3 which indicates that the receiver reverts back to the no-sync state and that the receiver awaits the initial flag (SOF) when in the no-sync state.

Regarding claims **3 and 49**, Trippe discloses processing in parallel a plurality of bits within said shift register to detect at least one stuff bit (see paragraph 39 on page 3); and discarding said at least one stuff bit, if detected (again, see paragraph 39 on page 3), wherein said valid payload data bits comprise all bits shifted into said shift register between said SOF sequence and said EOF sequence, excluding said at least one stuff bit (see paragraphs 37-38 and 40 on page 3 which indicates how the received data is that which is received between the start or end flags).

Regarding claim **4**, Trippe discloses discarding all bits received between said SOF and EOF sequences if an amount of valid payload data bits received constitute less than a minimum number (N) of bytes (see paragraph 41 on page 3 which indicates that the accumulator outputs the unframed (destuffed) bits in n-bit batches; clearly, if less than this number of bits is stored in the accumulator when a framing byte is detected, these bits are discarded since the accumulator only outputs n-bit batches).

Regarding claim **5**, the above combination of Trippe and Stevenson, Jr., as applied to claim 47 discloses the limitation of providing a plurality of comparators coupled to said shift register, wherein each comparator is coupled to said shift register so as to parallel process a unique combination of eight successive bits contained within said shift register.

Regarding claim **7**, Trippe discloses the limitation of searching for a specified sequence of bits stored within said shift register during a first clock cycle in paragraphs 9 and 10 on page 1, for example. See also lines 3-5 in paragraph 25 on page 2 which indicates that the processing of the multiple bits occurs in a single clock cycle.

Regarding claim **8**, Trippe discloses the limitation of searching for a start sequence within said shift register, wherein said valid payload data bits comprise at least some bits received after said start sequence in paragraph 35 of page 3, for example; the "start-of-frame" is the start sequence referred to in the claim. See also paragraphs 37-38 and 40 on page 3 which indicate how the received data is that which is received between the start or end flags, and thus after the start sequence.

Regarding claim **9**, Trippe discloses the limitation of searching for an end sequence within said shift register, after said start sequence has been detected, during at least one clock cycle subsequent to said first clock cycle, wherein said valid payload data bits comprise at least some bits received between said start and end sequences in paragraph 35 of page 3, for example; the "end-of-frame" is the end sequence referred to in the claim. See also paragraphs 37-38 and 40 on page 3 which indicate how the received data is that which is received between the start or end flags, and thus after the start sequence.

Regarding claim **10**, Trippe discloses the limitation that said bit-synchronous data comprises bit-synchronous HDLC data (see title and lines 1-5 of paragraph 23 on page 2), said start sequence comprises a SOF sequence and said end sequence comprises an EOF sequence in paragraph 35 of page 3, for example; the "start-of-frame" is the SOF sequence and "end-of-frame" is the EOF sequence.

Regarding claim **11**, Trippe discloses the limitation of processing in parallel a plurality of bits stored in said shift register to detect an Abort sequence during at least one clock cycle subsequent to said first clock cycle, wherein if said Abort sequence is detected, all bits received after said SOF sequence are discarded and a search for a new SOF sequence is initiated in paragraph 38 on page 3 which indicates that the receiver reverts back to the no-sync state and that the receiver awaits the initial flag (SOF) when in the no-sync state.

Regarding claim **12**, Trippe discloses the limitation of processing in parallel a plurality of bits within said shift register to detect at least one stuff bit (see paragraph 39 on page 3); and discarding said at least one stuff bit, if detected (again, see paragraph 39 on page 3), wherein said valid payload data bits comprise all bits shifted into said shift register between said SOF sequence and said EOF sequence, excluding said at least one stuff bit (see paragraphs 37-38 and 40 on page 3 which indicates how the received data is that which is received between the start or end flags).

Regarding claim **13**, Trippe discloses the limitation of discarding all bits received between said SOF and EOF sequences if an amount of valid payload data bits received constitute less than a minimum number (N) of bytes (see paragraph 41 on page 3 which indicates that the accumulator outputs the unframed (destuffed) bits in n-bit batches; clearly, if less than this

number of bits is stored in the accumulator when a framing byte is detected, these bits are discarded since the accumulator only outputs n-bit batches).

Regarding claim **14**, the above combination of Trippe and Stevenson, Jr., as applied to claim 47 discloses the limitation of providing a plurality of comparators coupled to said shift register, wherein each comparator is coupled to said shift register so as to parallel process a unique combination of eight successive bits contained within said shift register.

7. Claims **37- 46, and 50** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication 2002/0176449 to Trippe in view of U.S. Patent 5,081,654 to Stephenson, Jr. et al and in further view of U.S. Patent 5,465,345 to Blanc et al.

Regarding claim **37**, Trippe discloses a system for parallel processing bit-synchronous data (see lines 1-5 of paragraph 23 on page 2), comprising: a register for storing a plurality of bits of bit-synchronous data that comprises bit-synchronous HDLC data, said register stores at least two bytes of said bit-synchronous HDLC data (lines 6-8 of paragraph 26 on page 2 and figure 2, for example, which indicates that 16 or more bits are stored and processed at once); a de-framer unit (the flag/abort detector 330 of figure 5, for example), coupled to said shift register, for detecting valid payload data, wherein said de-framer unit processes in parallel a plurality of bits within said shift register during a first clock cycle (see lines 3-5 in paragraph 25 on page 2 which indicates that the processing of the multiple bits occurs in a single clock cycle) and searches for a start sequence comprised of a SOF sequence and an end sequence within said shift register (see lines 9-12 of paragraph 7 on page 1 and paragraph 35 of page 3, for example; the "start-of-frame" is the SOF sequence referred to in the claim), and said valid payload data

bits comprise at least some bits received between said SOF and EOF sequences (see paragraphs 37-38 and 40 on page 3 which indicates how the received data is that which is received between the start or end flags); and a packer logic unit, coupled to said de-framer unit, for storing said valid payload data received from said de-framer unit (bit accumulator 338 and bit shifter 336 in figure 5).

Similarly, regarding claim **44**, Trippe discloses a bit-synchronous HDLC engine (see title and lines 1-5 of paragraph 23 on page 2), comprising: a register for storing at least two bytes of bit-synchronous HDLC data (lines 6-8 of paragraph 26 on page 2 and figure 2, for example, which indicates that 16 or more bits are stored and processed at once); and a de-framer unit (the flag/abort detector 330 of figure 5, for example), coupled to said shift register, for detecting valid payload data within said shift register, said de-framer unit detects a SOF sequence during said first clock cycle (see lines 9-12 of paragraph 7 on page 1 and paragraph 35 of page 3, for example; the "start-of-frame" is the SOF sequence referred to in the claim; see also lines 3-5 in paragraph 25 on page 2 which indicates that the processing of the multiple bits occurs in a single clock cycle) and detects an EOF sequence during a subsequent clock cycle (see lines 9-12 of paragraph 7 on page 1 and paragraph 35 of page 3, for example; the "end-of-frame" is the EOF sequence referred to in the claim; see also lines 3-5 in paragraph 25 on page 2 which indicates that the processing of the multiple bits occurs in a single clock cycle), wherein said valid payload data comprises at least some of the bits received between said SOF sequence and said EOF sequence (see paragraphs 37-38 and 40 on page 3 which indicates how the received data is that which is received between the start or end flags), and said de-framer unit further processes in parallel a plurality of bits within said shift register to detect at least one stuff bit and discards said

at least one stuff bit, if detected (see paragraph 39 on page 3), wherein said valid payload data bits comprise all bits shifted into said shift register between said SOF sequence and said EOF sequence (see paragraphs 37-38 and 40 on page 3 which indicates how the received data is that which is received between the start or end flags), excluding said at least one stuff bit (paragraphs 39 and 41 on page 3 indicate that the valid data forwarded does not include the stuff bits); and a packer logic unit, coupled to said de-framer unit, for storing said valid payload data received from said de-framer unit (bit accumulator 338 and bit shifter 336 in figure 5).

Trippe does not disclose expressly the limitation that the HDLC data is stored in a shift register, wherein, at each successive clock cycle, a new incoming byte is shifted into said shift register and an old byte is shifted out of said shift register of claims 37 and 44. Trippe does not disclose the limitation of claims 37 and 44 that said de-framer unit comprises a plurality, of comparators for detecting a specified sequence of bits within said shift register during a first clock cycle, wherein each comparator is coupled to a unique subset of eight successive bits contained within said shift register. Finally, Trippe does not disclose expressly the limitation that said de-framer unit further comprises a look-up table (LUT) representing a plurality of bit sequences containing at least one stuff bit, wherein, if a stuff bit is detected, said LUT passes through valid payload data bits while not allowing said at least one stuff bit to be sent to said packer logic unit.

Stevenson, Jr. discloses the limitations of claims 37 and 44 of a shift register wherein at each successive clock cycle, a new incoming byte is shifted into said shift register and an old byte is shifted out of said shift register in lines 9-24 of column 6. Specifically, the passage starting on line 15 indicates that each data word causes the previous data words to be shifted over

one latch. Stevenson, Jr. further discloses the limitation that the de-framer unit comprises a plurality, of comparators for detecting a specified sequence of bits within said shift register during a first clock cycle, wherein each comparator is coupled to a unique subset of eight successive bits contained within said shift register in lines 24-49 of column 6 and in the example of figure 6. Clearly, successive 8-bit sequences of bits are scanned simultaneously to detect a given word (framing byte in this case).

Trippe and Stevenson, Jr. are analogous art because they are from the same field of endeavor of detecting byte patterns in bit sequences. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Trippe by using the shift registers (latches) to store the HDLC data while it is being analyzed and to further use the detectors as described by Stevenson, Jr. to simultaneously look at all successive 8-bit sequences in this shift register.

The motivation for doing so would have been allow the 8-bit framing bytes (SOF, EOF) to be detected regardless of the starting bit location of that byte as suggested by Stevenson, Jr. in lines 44-49 of column 6.

The combination of Trippe and Stevenson, Jr. does not disclose expressly the limitation that said de-framer unit further comprises a look-up table (LUT) representing a plurality of bit sequences containing at least one stuff bit, wherein, if a stuff bit is detected, said LUT passes through valid payload data bits while not allowing said at least one stuff bit to be sent to said packer logic unit.

Blanc discloses a look-up table (LUT) representing a plurality of bit sequences containing at least one stuff bit, wherein, if a stuff bit is detected, said LUT passes through valid payload

data bits while not allowing said at least one stuff bit to be sent to said packer logic unit in lines 25-38 of column 2 and lines 6-12 of column 8 which describe the zero delete table which is used to remove stuffed zeros from the HDLC stream.

Trippe, modified by Stevenson, Jr., and Blanc are analogous art because they are from the same field of endeavor of HDLC bit stream processing. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Trippe, modified above, to further use a look up table such as the zero delete table in Blanc. The motivation for doing so would have been to provide faster processing as well as lower cost as suggested by Blanc in lines 33-38 of column 2. Therefore, it would have been obvious to combine Blanc with Trippe and Stevenson, Jr. for the benefit of faster processing and lower cost to obtain the invention as specified in claims 37 and 44.

Regarding claim **38**, Trippe discloses discarding all bits received between said SOF and EOF sequences if an amount of valid payload data bits received constitute less than a minimum number (N) of bytes (see paragraph 41 on page 3 which indicates that the accumulator outputs the unframed (destuffed) bits in n-bit batches; clearly, if less than this number of bits is stored in the accumulator when a framing byte is detected, these bits are discarded since the accumulator only outputs n-bit batches).

Regarding claim **39**, Trippe discloses the limitation of searching for a specified sequence of bits stored within said shift register during a first clock cycle in paragraphs 9 and 10 on page 1, for example. See also lines 3-5 in paragraph 25 on page 2 which indicates that the processing of the multiple bits occurs in a single clock cycle.

Regarding claim **40**, Trippe discloses the limitation of searching for a start sequence within said shift register, wherein said valid payload data bits comprise at least some bits received after said start sequence in paragraph 35 of page 3, for example; the "start-of-frame" is the start sequence referred to in the claim. See also paragraphs 37-38 and 40 on page 3 which indicate how the received data is that which is received between the start or end flags, and thus after the start sequence.

Regarding claim **41**, Trippe discloses the limitation of searching for an end sequence within said shift register, after said start sequence has been detected, during at least one clock cycle subsequent to said first clock cycle, wherein said valid payload data bits comprise at least some bits received between said start and end sequences in paragraph 35 of page 3, for example; the "end-of-frame" is the end sequence referred to in the claim. See also paragraphs 37-38 and 40 on page 3 which indicate how the received data is that which is received between the start or end flags, and thus after the start sequence.

Regarding claims **42 and 46**, Trippe discloses processing in parallel a plurality of bits within said shift register to detect an Abort sequence during said at least one subsequent clock cycle, wherein if said Abort sequence is detected, all bits received after said SOF sequence are discarded and a search for a new SOF sequence is initiated in paragraph 38 on page 3 which indicates that the receiver reverts back to the no-sync state and that the receiver awaits the initial flag (SOF) when in the no-sync state.

Regarding claim **43**, Trippe discloses processing in parallel a plurality of bits within said shift register to detect at least one stuff bit (see paragraph 39 on page 3); and discarding said at least one stuff bit, if detected (again, see paragraph 39 on page 3), wherein said valid payload

data bits comprise all bits shifted into said shift register between said SOF sequence and said EOF sequence, excluding said at least one stuff bit (see paragraphs 37-38 and 40 on page 3 which indicates how the received data is that which is received between the start or end flags).

Regarding claim **45**, Trippe discloses a packer logic unit, coupled to said de-framer unit, for storing said valid payload data received from said de-framer unit (bit accumulator 338.and bit shifter 336 in figure 5), wherein said packer logic unit discards said valid payload data received from said de-framer unit if an amount of valid payload data bits received constitute less than a minimum number (N) of bytes (see paragraph 41 on page 3 which indicates that the accumulator outputs the unframed (destuffed) bits in n-bit batches; clearly, if less than this number of bits is stored in the accumulator when a framing byte is detected, these bits are discarded since the accumulator only outputs n-bit batches).

Regarding claim **50**, the combination of Trippe and Stevenson, Jr. discloses the limitations of parent claim 47 as disclosed above. The combination of Trippe and Stevenson, Jr. does not disclose expressly the limitation of claim 50 that said de-framer unit further comprises a look-up table (LUT) representing a plurality of bit sequences containing at least one stuff bit, wherein, if a stuff bit is detected, said LUT passes through valid payload data bits while not allowing said at least one stuff bit to be sent to said packer logic unit.

Blanc discloses a look-up table (LUT) representing a plurality of bit sequences containing at least one stuff bit, wherein, if a stuff bit is detected, said LUT passes through valid payload data bits while not allowing said at least one stuff bit to be sent to said packer logic unit in lines

25-38 of column 2 and lines 6-12 of column 8 which describe the zero delete table which is used to remove stuffed zeros from the HDLC stream.

Trippe, modified by Stevenson, Jr., and Blanc are analogous art because they are from the same field of endeavor of HDLC bit stream processing. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Trippe, modified above, to further use a look up table such as the zero delete table in Blanc. The motivation for doing so would have been to provide faster processing as well as lower cost as suggested by Blanc in lines 33-38 of column 2. Therefore, it would have been obvious to combine Blanc with Trippe and Stevenson, Jr. for the benefit of faster processing and lower cost to obtain the invention as specified in claim 50.

8. Claim **15** is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication 2002/0176449 to Trippe in view of U.S. Patent 5,081,654 to Stephenson, Jr. et al and in further view of U.S. Patent 6,970,563 to Risling.

The combination of Trippe and Stevenson, Jr. discloses the limitations of parent claim 47 as disclosed above. The combination of Trippe and Stevenson, Jr. does not disclose expressly the limitation of claim 15 of de-scrambling said at least two bytes prior to storing said at least two bytes in said shift register, wherein said de-scrambling comprises de-scrambling at least eight bits in parallel during a single clock cycle.

However, Risling discloses this limitation in Figure 7 and lines 4-25 of column 7. Lines 4-7 indicate that in this embodiment, 32 bits are descrambled in parallel. Trippe, modified as above, and Risling are analogous art because they are from the same field of endeavor of fast

(parallel) processing of serially transmitted data. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the above combination of Trippe and Stevenson, Jr. by descrambling the data stream prior to performing HDLC processing. The motivation for doing so would have been to allow the receiver to handle scrambled data in order to overcome the problems associated with sending an unbalanced number of 0s and 1s as well as to make the data unintelligible in case it is intercepted. This is suggested in lines 24-44 of column 1 of Risling. Therefore, it would have been obvious to combine Risling with Trippe as modified by Stevenson, Jr. for the benefit of receiving scrambled data to obtain the invention as specified in claim 15.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- U.S. Patent 6,674,770 to Jarfjord discloses a method of bit stuffing for synchronous HDLC.
- U.S. Patent 5,119,478 to Calvignac et al discloses a method for parallel processing HDLC bit streams.
- U.S. Patent 6,898,647 to Duvvuru discloses parallel byte processing engines shared among multiple data channels.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert C. Scheibel whose telephone number is 571-272-3169. The examiner can normally be reached on Monday and Thursday from 6:30-5:00 Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema S. Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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